AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to Figures 2 and 3.

Attachment: Replacement sheet

Annotated sheet showing changes

REMARKS

Claims 1-10 were pending in the application. By this amendment, claims 8 and 9 are canceled. New claims 11-17 have been added. Claims 8 and 9 have been canceled without disclaimer or prejudice to allow claims 11-17 to be added without additional fee.

As a result of the amendment, claims 1-7 and 10-17 are pending in the application. Claims 1, 10 and 11 are independent.

In the Drawings

The Examiner has objected to FIGS. 2 and 3 because the legend does not indicate the figures show the prior art. The enclosed replacement sheet should remove this objection.

Oath/Declaration

The Examiner has objected to the Declaration because it does not show a mailing address of the inventors. Concurrently with this amendment, the Applicants have submitted a Supplemental Application Data Sheet indicating the mailing addresses of the inventors. The Application Data Sheet should remove this objection.

Claims Rejections under 35 U.S.C. §112

Claims 3, 4 and 7 are rejected as reciting a bus layout file created as part of generating test signals. Applicants have amended claim 3 (and therefore claims 4 and 7, which depend from claim 3) to indicate that the bus layout file is created as part of generating test program information.

This approach is described in paragraphs 22 and 23 of the published application and is shown as step 100 in FIG. 5. Accordingly, the claims as now amended are supported by the specification.

Claim 5 is rejected under 35 U.S.C. §112 because producing a list of packet and control entities is not described in the specification to be part of generating test signals. Claim 5 has also been amended to indicate that producing a list of packet and control entities occurs as part of generating test program information. These steps are, for example, described at paragraph 24 of the published application and shown as step 104 of FIG. 5.

Claims 6 is rejected under 35 U.S.C. §112, second paragraph. The rejection is premised on the rejections of claims 3-5 and 7. However, claim 6 does not depend from any of the claims otherwise rejected under 35 U.S.C. §112 and such a rejection is not proper.

A brief overview of the specification and a comparison to the cited references may aid the Examiner in recognizing that claim 6 clearly defines subject matter for which protection is sought.

The present application describes testing semiconductor devices in which multiple subcircuits may be connected to an output pin through a communications port (See FIG. 2). During operation of the semiconductor device, each of the subcircuits may operate subject to timing variations. Because each of the subcircuits operates independently, each may be subject to a different timing variation.

FIG. 3 illustrates a problem that can arise because of these timing variations. On the left side of FIG. 3, an expected sequence of values at the output pin is illustrated. That sequence is shown to contain sub-parts labeled "Packet 1," "Packet 2" and "Packet 3." In this illustration, each of the sub-parts is generated by one of the subcircuits shown in FIG. 2. If, because of the timing variations, Subcircuit #3 generates Packet 3 earlier than expected and/or Subcircuit #2 generates Packet 2 later than expected, the actual sequence of output values may appear as shown on the right of FIG. 3. In that example, the order of Packet 3 and Packet 2 is reversed.

If the timing variations that cause the order of Packet 2 and Packet 3 to be reversed are within the normal operating limits of the device under test, the device should not be identified as a bad device, even though the actual output, shown on the right in FIG. 3, does not match the expected output, shown on the left in FIG. 3. Accordingly, the application describes a method and apparatus to test a device so that even in the conditions depicted in FIG. 3, the device will not be deemed a faulty device. This result is in contrast to the testers of Schinabeck and Miura that would indicate a device failure because the actual output sequence does not match the expected output sequence.

Schinabeck et al. describes an automated test system in which a "pass window" may be defined. The "pass window" relates to a range of allowed values that a signal may have when measured. At column 18, starting at line 13, Schinabeck describes how the pass window current limits are defined. These limits apply to a single signal. If the signal, when measured, has a current outside this range, it is deemed to fail. If the condition illustrated in FIG. 3 of the present application cause the sub-parts of the actual output to not match the sub-parts of the expected value sequence, the tester of Schinabeck will deem the part a "fail." The "pass window" in Schinabeck does not avoid this problem.

Rivoir also relates to measurements on a single signal and it, too, will not indicate the desired test result when the situation pictured in FIG. 3 of the present application occurs. In Rivoir, transitions in a signal are represented by "time stamps." (Paragraph 41). The time stamps generated from the transitions in a signal under test form a time stamp sequence. The time stamp sequence can be compared to an expected sequence of time stamps. Comparing the time stamp sequences generated for a signal under test and an expected output signal is analogous to comparing the actual signals. (Paragraph 50). Rivour does not use the term "window," but even if a window were applied to the time stamps, the resulting system would not produce the desired result when sub-parts of a sequence are out of order.

In contrast to the prior art, the tester in the application processes the output sequence in sub-parts, such as the packets illustrated in FIG. 3. Each sub-part in the actual output sequence

must match a sub-part in the expected output sequence. However, the sub-parts in the actual output sequence need not appear in the exact order in which they appear in the expected output sequence. Rather, the application describes that information about a device under test may be used to determine a "window" in the expected output sequence. If a sub-part of the actual output sequence matches a sub-part in its window, the expected output is deemed to have occurred, even though the sub-parts of the actual output sequence are not ordered in the same way as the sub-parts of the expected output sequence.

In the example of FIG. 5 of the present application, comparison between the actual and expected outputs is made by first comparing the actual output sequence to the expected output sequence as in a conventional test system. If the comparison matches, processing proceeds from decision block 110 to block 112, indicating that the device passed the test.

However, if the expected output sequence does not match the actual output sequence, the device is not immediately deemed to fail as in the prior art. Rather, the test continues to block 116. As indicated at block 116, each of the sub-parts in the actual output sequence is compared to a list of valid expected sub-parts. The list of valid expected sub-parts may define a "window." In this way, the actual output may be deemed to match the expected output even if the sub-parts in the actual output are not in the same order as the entities in the expected output.

Claim 6 is consistent with the specification and is clear to one of skill in the art in light of the specification. In the example of FIG. 5, the sub-parts of the output sequence are described as "entities," which is a term used in the claim. Claim 6 depends from claim 1, which defines steps that include capturing output entities and comparing the actual output entities to a window of expected output entities, all of which are consistent with the examples provided in the specification. Claim 6 recites in more detail the construction of an entity. These details are also consistent with the application, being shown, for example, in FIG. 3 of the application. Accordingly, the rejection under 35 U.S.C. §112, second paragraph, should be withdrawn.

Claim Rejection under 35 U.S.C. §102

The Examiner has rejected claims 1, 8 and 10 as being anticipated by Schinabeck et al. Applicants respectfully disagree.

As noted above, Schinabeck describes a test system in which a window of allowed current values is defined. Specific signals are tested to determine whether they have a value within this range. However, the reference does not relate to processing output signals as entities or to processing captured values so that, if entities appear out of order, the device does not improperly fail a test. Therefore, Schinabeck neither teaches nor suggests multiple limitation of claim 1. For example, the reference does not teach "capturing actual output entities." Nor does the reference describe "defining a window of valid expected entities" that is used for "comparing the failed actual output entity." Accordingly, the rejection of claim 1 should be withdrawn.

Claim 10 contains similar language and the rejection of claim 10 should be similarly withdrawn.

Claim Rejections under 35 U.S.C. §103

Claims 1, 2 and 8-10 are rejected as obvious over Miura in view of Rivoir. Applicants respectfully disagree. Even if Miura and Rivoir were combined, the combination would not meet the limitations of the claims.

As noted by the Examiner, Miura does not disclose "defining a window of valid expected entities" if a failure is identified and "comparing the failed actual output entity to the window." Rivoir does not teach or suggest adding such a limitation to the system of Miura.

Rivoir describes representing both an actual output signal and an expected output signal by a sequence of time stamps. However, Rivoir does not mention the possibility that the signals

giving rise to the time stamps may occur out of the expected order. Nor does Rivoir otherwise teach or suggest "defining a window of valid expected entities" and "comparing the failed actual output entity to the window." Accordingly, even if Miura and Rivoir were combined, the combination would not teach or suggest every limitation of claim 1, and the rejection under 35 U.S.C. §103 should be withdrawn.

Claim 10 contains similar limitations and the rejection of claim 10 should be withdrawn for similar reasons.

Claim 2 depends from claim 1 and should be allowed for the reasons given above in connection with claim 1. Claim 2 defines a process step that occurs following the comparison of the failed actual output entity to the window. Because neither Miura nor Rivoir teaches or suggests a comparison of a failed actual output entity to a window of valid expected entities, neither reference could teach or suggest processing following such a comparison.

Though claims 3-7 were not considered by the Examiner, they likewise depend from claim 1 and should be allowed for the reasons given above in connection with claim 1.

Newly added claims 11-17 also recite features of the system described in the present application that are not shown or suggested in the references. Specifically, the claims describe actual values and expected values that are both represented by ordered sequences with sub-parts. A match is indicated when a sub-part of the actual values matches a "sub-part of the second plurality of ordered sub-parts" that is "offset by less than a number of sub-parts from a corresponding sub-part." The claim expressly states that this "number" defining the offset is greater than 1. Because none of the references teaches or describes matching sub-parts of a sequence of values to sub-parts offset from a corresponding sub-part, none of the references teaches or suggests the method of claims 11-17. Accordingly, those claims should likewise be allowed.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 23/2825, under Order No. T0529.70057US00 from which the undersigned is authorized to draw. If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated:

Respectfully submitted,

By

Edmund J. Walsh
Registration No.: 32,950
WOLF, GREENFIELD & SACKS, P.C.
Federal Reserve Plaza
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
(617) 646-8000

Attachments

OIPE MPT7
MAY 02 2006
PATENT & TRADEMARK OFFICE

FIG. 2
(PRIOR ART)

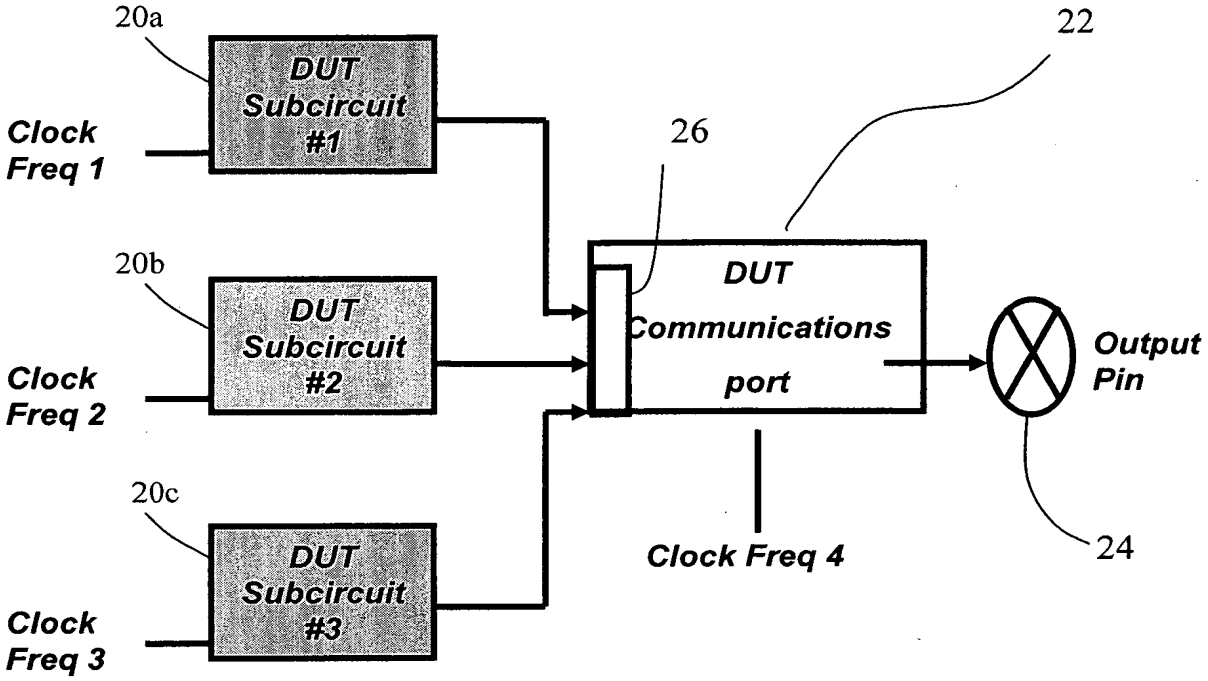

FIG. 3
(PRIOR ART)